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PATENT APPLICATION

ATTORNEY DOCKET NO. 10971798-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Dave Goh, et al.

Confirmation No.: 1530

Application No.: 09/102,207

Examiner: David Donald Davis

Filing Date: June 22, 1998

Group Art Unit: 2627

Title: WEB SERVER CHIP FOR NETWORK MANAGEABILITY

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDED

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 2, 2005.

~~The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00~~.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ ~~500~~ 0. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Date of facsimile:
Typed Name: Douglas L. Weller
Signature: Douglas L. Weller

Respectfully submitted,

Dave Goh, et al.

By Douglas L. Weller

Douglas L. Weller

Attorney/Agent for Applicant(s)

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Date : April 27, 2006

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INVENTOR(S): Dave Goh, et al.

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FILED: June 22, 1998 **EXAMINER:** David Donald Davis

SUBJECT: WEB SERVER CHIP FOR NETWORK MANAGEABILITY

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

AMENDED APPEAL BRIEF

Appellant herein sets forth his reasons and arguments for appealing the Examiner's final rejection of claims in the above-identified case.

REAL PARTY IN INTEREST

This Patent Application has been assigned to Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having it principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Appellant is aware of no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 41 are extant in the case.

Claims 31 through 41 have been withdrawn from consideration.

Claims 1 through 30 are rejected.

The appealed claims are claims 1 through 30.

STATUS OF AMENDMENTS

After the final rejection, Appellant filed a Response to Office Action dated February 16, 2005. In the Response to Office Action, no amendments were made to the claims.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1:

Claim 1 sets out a chip (38) for incorporation within a network device (18) that is connectable to a computer network (20,22,24,34). The network device (18) includes a host processor (40). See Figure 1 and the Specification at page 4, line 18 through page 5, line 2.

The chip (38) includes a media access controller (42), a host interface (52-54) and an embedded processor (48). The media access controller (42) is connectable to the computer network (20,22,24,34). The media access

controller (42) provides the chip (38) with access to the computer network (20,22,24,34) independent of the host processor (40). See Figure 3 and the Specification at page 7, line 23 through page 8, line 10.

The host interface (52-54) is connectable to the host processor (40). See Figure 3, and the Specification at page 8, line 22 through page 10 line 4.

The embedded processor (48) is coupled between the host interface (52-54) and the media access controller (42). The embedded processor (48) is programmable to function as a manageability web server, communicate with the host interface (52-54) and obtain manageability information about the network device (18). The embedded processor (48) is also programmable to send the manageability information to the media access controller (42) for transmission over the computer network (20,22,24,34). In this way, the chip (38) performs network management functions independent of the host processor (40). See Figure 3 and the Specification at page 11, line 12 through page 12, line 3.

Claim 13:

Claim 13 sets out network device (18) connectable to a computer network (20,22,24,34). The network device (18) includes interchip communications means (70), a compliant device (74), a chip (38) and non-volatile memory (68). The compliant device (74) is coupled to the interchip

communications means (70). See Figure 3 and the Specification at page 12, line 24 through page 13, line 5.

The chip (38) includes a media access controller (42) connectable to the computer network (20,22,24,34), an interchip communications interface (72) connected to the interchip communications means (70), and an embedded processor (48) coupled to the interchip communications interface (72) and the media access controller (42). See Figure 3 and the Specification at page 13, lines 1 through 20.

The non-volatile memory (68) is programmed with a plurality of executable instructions. The instructions, when executed, instruct the embedded processor (48) to function as a manageability web server, communicate with the interchip communications means (70) to obtain manageability information about the compliant device (74), and send the manageability information to the media access controller (42) for transmission over the computer network (20,22,24,34). See Figure 3 and the Specification at page 11, line 12 through page 12, line 12 and at page 10, lines 10 through 17.

Claim 23:

Claim 23 sets out a system comprising a computer network, a network device and a network manager. The network device (18) includes a host processor (40) and a chip (38). See Figure 1 and the Specification at page 4, line 18 through page 5, line 2.

The chip (38) includes a media access controller (42) and an embedded processor (48). The media access controller (42) is coupled to the computer network (20,22,24,34). The embedded processor (48) is coupled to the media access controller (42) and programmed to function as an HTTP manageability web server. See the Specification at page 12, lines 4 through 12.

The network manager (30) is coupled to the computer network (20,24,34). The network manager (30) includes a web browser and a plurality of HTML files for instructing the network manager (30) to communicate with the embedded processor (48) in the network device (18) and perform network management of the network device (18). In this way, the embedded processor (48) can communicate with the network manager (30) independent of the host processor (40). See the Specification at page 11, lines 12 through 23.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 1 through 3, 5, 6, 8, 12 through 15, and 19 through 20 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by USPN 6,532,497 (*Cromer*).

(2) Claims 7, 9 through 11, 18 and 21 through 30 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over *Cromer*.

(3) Claims 4, 16 and 17 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over *Cromer* in view of USPN 5,903,737 (*Han*).

ARGUMENT

Rejection of Claims under 35 U.S.C. § 102(e)

A. Overview specifying errors in the rejection of the claims.

The criteria for a rejection under 35 U.S.C. § 102 has been clearly defined by the courts and confirmed by the U.S. Patent and Trademark Office. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner has failed to show that each and every element set forth in the independent claims is found either expressly or inherently in *Cromer*.

Below, Appellant clearly and unambiguously points out subject matter within each independent claim that is not disclosed or suggested by *Cromer*. On the basis of this, Appellant believes all the claims are patentable over *Cromer*.

B. Description of *Cromer*.

Cromer discloses a separately powered network interface for reporting the activity states of a network connected client.

Figure 5 of *Cromer* shows an implementation of logic 400, used to collect selected system information. See *Cromer* at column 1, lines 35 through 38. The logic 400 monitors logic signals from client system 104, detects states, creates

packets, and sends data over the MII bus to physical layer 304. See *Cromer* at column 3, lines 44 through 47.

Within logic 400 a non-volatile memory 504 is shown. The non-volatile memory 504 is used to store information for packet generation such as IP header, UDP header and universal identifier (UUID). See *Cromer* at column 3, lines 55 through 59.

C. Discussion of Independent Claim 1.

1. Subject matter within independent claim 1 not disclosed by *Cromer*.

Independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor. The embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network.

Cromer does not disclose or suggest an embedded processor being programmable to function as a manageability web server, as set out in claim 1.

Cromer does not disclose or suggest an embedded processor being programmable to send manageability information to a media access controller for transmission over the computer network, as set out in claim 1.

2. Errors made by the Examiner in the stated rationale for the rejection.

The Examine has failed to correctly ascertain the disclosed subject matter of *Cromer*. This has led to an incorrect rejection of independent claim 1 over *Cromer*. Below, Appellant specifically responds to incorrect assertions made by the Examiner pertaining to the disclosed subject matter in *Cromer*.

a. Response to the Examiner's argument that in *Cromer* the logic 400 is programmable to function as a manageability web server.

The Examiner has asserted: "*Cromer* et al discloses in column 3, lines 32-52 that the embedded processor 400 is programmable to function as a manageability web server..." See the Office Action *mailed* January 12, 2005 at page 3, lines 5 through 7. This statement by the Examiner is incorrect.

> *Cromer* at column 3, lines 44 through 47 states the following:
> The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 detects states, creates packets, and sends data over the MII bus to physical layer 304. This is the only functionality that *Cromer* discloses that is performed by logic 400. Nowhere does *Cromer* disclose or suggest that logic 400 is programmed to function as a manageability web server. In fact, nowhere does *Cromer* indicate that logic 400 is able to receive packets or any other communications over a network. Thus, it is clear that *Cromer* does not disclose or suggest logic is programmed to function as a manageability web server.

b. Response to the Examiner's argument that in *Cromer* the logic 400 is programmable to send manageability information to the media access controller 308 for transmission over the computer network.

The Examiner has asserted: "The embedded processor 400 further is programmable to send the manageability information to the media access controller 308 for transmission over the computer network." See the Office Action *mailed* January 12, 2005 at page 3, lines 7 through 9. This assertion by the Examiner is incorrect and has no foundation in the subject matter actually disclosed by *Cromer*.

For example, *Cromer* at column 3, lines 42 through 47 states the following:

> By so connecting the logic 400 at the MII bus, it can send network packets using the physical layer 304. The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 sends data to physical layer 304, not to the media access controller 308. While logic 400 and media access controller 308 are both connected to the MII bus, nowhere does *Cromer* give any disclosure or suggestion that logic 400 and media access controller ever communicate with each other.

There is therefore no disclosure or suggestion in *Cromer* that logic 400 is programmable to send manageability information to the media access controller 308 for transmission over the computer network. The Examiner's assertion to the contrary has no foundation in the subject matter actually disclosed by *Cromer*.

3. Reply to arguments Examiner made in the Examiner's Answer:

a. Manageability Web Servers

Examiner has argued in the Examiner's Answer at page 10 and 11, as follows:

> The *claimed invention* only requires the embedded processor to send manageability information for transmission over the computer network and perform network management functions independent of the host processor. The claims do not require the processor to received packets or any other communications over a network. However, assuming arguendo that the claimed *invention* does in fact require the processor to received packets or any other communications over a network. Figure 4 clearly shows bidirectional arrows indicating bidirectional communications (i.e. send and received packets and other communications) over the network. Therefore, contrary to appellant's incorrect interpretative conclusory statement, processor 400 of Cromer does function as a manageability web server, which is not unlike appellant's *claimed and disclosed invention.*
> ...Appellants statements in section D.2.a on page 11 are incorrect. Not only does Cromer show non-volatile memory 504 in figure 5, but Cromer shows microcontroller 502. Microcontrollers include a CPU core and memory (ROM or Flash memory, which is non-volatile memory) for the program, which is a plurality of executable instructions. (italics in the original)

Examiner essentially argues that logic 400 within Cromer acts as a manageability web server. This argument is made by Examiner without support from any language within Cromer that makes any suggestion that logic 400 disclosed by Cromer acts as a manageability web server or is even capable of acting as a web server.

As shown by Figure 5 of Cromer, logic 400 has relatively modest processing capability and there is no indication from Figure 5 (or any other information within Cromer) that would lead one of ordinary skill in the art to suppose that logic 400 is functioning as, or would be capable of functioning as, a

web server. While Examiner refers to logic 400 as "processor 400" this language is not utilized by Cromer. Cromer, recognizing the modest processing power of logic 400, utilizes the term "logic 400".

It is well understood by persons in the art that web servers require significant processing resources. For example, in Newton's Telecom Dictionary, The Official Dictionary of Telecommunication & the Internet, 15th Edition, Published by Miller Freeman, Inc., 1999, a Web Server is defined as "a powerful computer which connects to the Internet or an Intranet. It stores documents and files—audio, video, graphics or text—and can display them to people accessing the server via hypertext transfer protocol (http). A Web server derives its name because it is part of the World Wide Web."

Appellant does not rely on the above-cited definition, but is mentioning it merely as an example of what is commonly known and understood in the art about web servers. Appellant notes that a large percentage of the population of the United States, (and the world) utilize the internet, access web servers, and are familiar with what is meant by terms such as world wide web and web servers. No person of ordinary skill in the art would mistake logic 400, disclosed by Cromer, for a web server.

b. Reliance on Written Description of Cromer

Examiner has argued in the Examiner's Answer at page 10 and 11, as follows:

> In the action mailed January, 12, 2005 it was stated in response to the same assertion presented, supra, that Cromer in "figure 4 clearly shows data lines being bi-directional between embedded processor 400 and media access controller (MAC) 308 as required

> by the pending claims." It is curious that appellant has not traversed (i.e. a formal denial of one material fact that contradicts) the preceding statement. Appellant, however, has chosen to ignore the preceding statement and rely *solely* on the written specification, which appellant purports to be silent on processor 400 communicating with the MAC 308. The disclosure of Cromer includes more than the written specification. It also includes the drawings. The disclosure, specifically the drawings, contrary to appellants assertion, does in fact show and suggest processor 400 and MAC 308 communicating with each other. (italics in the original)

Examiner argues that Figure 4 of Cromer shows packet logic 400 communicating with media access controller (MAC) 308. Examiner relies on this premise to conclude that logic 400 is programmable to send manageability information to the media access controller 308 for transmission over the computer network.

Both Examiner's premise and conclusion are erroneous.

Examiner asserts that Cromer in figure 4 clearly shows data lines being bi-directional between embedded processor 400 and media access controller (MAC) 308. This is an incomplete and misleading description of what is shown in Figure 4. Figure 4 shows a bi-directional arrow extending from media access controller (MAC) 308 to physical layer 304. This bi-directional arrow is labeled MII (for MII bus). This connection (represented by a bi-directional arrow) of the physical layer 304 to MAC 304 through the MII bus is also shown in Figure 3 of Cromer, and illustrates the communication of MAC 308 with physical layer 304.

Figure 4, however, shows an additional arrow not included in Figure 3. Specifically, in Figure 4, an arrow has been added which points away from the middle of the bi-directional arrow that extends between MAC 308 and physical layer 304. This added arrow points to packet logic 400.

Cromer very specifically explains what this additional arrow (shown in Figure 4, but not Figure 3), represents. For example, *Cromer* at column 3, lines 42 through 47 states the following:

> By so connecting the logic 400 at the MII bus, it can send network packets using the physical layer 304. The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 sends data to physical layer 304, not to the media access controller 308.

This explanation for the existence of this additional arrow (shown in Figure 4, but not Figure 3), given within the written specification of Cromer, is a complete explanation for the existence of the additional arrow (shown in Figure 4, but not Figure 3).

Examiner has ignored this specific explanation given by Cromer for the existence of this additional arrow (shown in Figure 4, but not Figure 3), and instead has chosen to assign functionality to this arrow (shown in Figure 4, but not Figure 3) which is neither taught by Cromer nor is in any way compatible with the teaching of Cromer. This is not a fair reading of what is taught by Cromer, but rather is a reading into Cromer of information that is not taught by Cromer and is incompatible with the written disclosure of Cromer.

D. Discussion of Independent Claim 13.

1. Subject matter within independent claim 13 not disclosed by *Cromer*.

Independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip

communications interface and an embedded processor. Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network.

Cromer does not disclose or suggest a non-volatile memory programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server, and send manageability information to a media access controller for transmission over the computer network.

2. Errors made by the Examiner in the stated rationale for the rejection.

The Examiner has failed to correctly ascertain the disclosed subject matter of *Cromer*. This has led to an incorrect rejection of independent claim 13 over *Cromer*. Below, Appellant specifically responds to incorrect assertions made by the Examiner pertaining to the disclosed subject matter in *Cromer*.

a. Response to the Examiner's argument that in *Cromer* non-volatile memory 504 is programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server.

The Examiner has asserted the following:

> Figure 5, in particular, of *Cromer* et al shows non-volatile memory programmed with a plurality of executable instructions (source, destination, length, etc.). The instructions, when executed, instructing the embedded processor 400 to function as a

> manageability web server, communicate with the interchip communication to obtain manageability information about the compliant device and send the manageability information to the media access controller 308 for transmission over the computer network.

See the Office Action mailed January 12, 2005 at page 4, lines 7 through 9.

The assertion by the Examiner that non-volatile memory 504 is programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server is clearly incorrect and has no basis in the disclosure or teaching of *Cromer*.

> *Cromer* at column 3, lines 55 through 59 states the following: When timer 508 expires, microcontroller 502 according the invention will gather information for packet generation such as IP header, UDP header and universal identifier (UUID) from non-volatile memory 504.

This is the only information *Cromer* discloses about non-volatile memory 504. Nothing in *Cromer* discloses or suggests that non-volatile memory is programmed with a plurality of executable instructions, the instructions, when executed, instructing an embedded processor to function as a manageability web server, as set out in claim 13 of the present case.

b. Response to the Examiner's argument that in *Cromer* non-volatile memory 504 is programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to send manageability information to a media access controller for transmission over a computer network.

The Examiner has asserted the following:

> Figure 5, in particular, of *Cromer* et al shows non-volatile memory programmed with a plurality of executable instructions (source, destination, length, etc.). The instructions, when executed, instructing the embedded processor 400 to ... send the manageability information to the media access controller 308 for transmission over the computer network.

See the Office Action *mailed* January 12, 2005 at page 4, lines 7 through 9. This assertion by the Examiner is incorrect and has no foundation in the subject matter actually disclosed by *Cromer*.

For example, *Cromer* at column 3, lines 42 through 47 states the following:

> By so connecting the logic 400 at the MII bus, it can send network packets using the physical layer 304. The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 sends data to physical layer 304, not to the media access controller 308. While logic 400 and media access controller 308 are both connected to the MII bus, nowhere does *Cromer* give any disclosure or suggestion that logic 400 and media access controller ever communicate with each other. This is a clear teaching away from the subject matter set out in claim 1 of the present case.

Rejection of Claims under 35 U.S.C. § 103(a)

A. Overview Specifying Errors in the Rejection of the Claims.

The U.S. Patent and Trademark Office has set forth a methodology for establishing a *prima facie* case of obviousness. Specifically three basic criteria must be met.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP 706.02 (j).

Appellant believes the Examiner has failed to establish a *prima facie* case of obviousness for the claims extant in the present case because there are claim limitations that are not taught or suggested by *Cromer* and/or *Han*. Below, Appellant discusses the independent claim rejected under 35 U.S.C. § 103(a). On the basis of the allowability of the independent claims, Appellant believes all the claims are patentable over the cited art.

B. Discussion of Independent Claim 23

1. Subject matter within independent claim 23 not disclosed by *Cromer*.

Independent claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. *Cromer* does not disclose or suggest a chip including an embedded processor programmed to function as an HTTP manageability web server.

a. Response to the Examiner's argument that in *Cromer* the logic 400 can be programmed to function as a manageability web server.

The Examiner has asserted the following: "In column 1, lines 40 through 44 of *Cromer* et al discloses that processor 400 can be programmed to function as a manageability web server and a network manager coupled to the computer network." See the Office Action mailed January 12, 2005, at page 6, lines 7 through 9. This statement by the Examiner is incorrect. In column 1, lines 40 through 44, *Cromer* discusses prior art software available to manage systems remotely. In column 1, lines 40 through 44, *Cromer* is not discussing logic 400.

Nothing in column 1, lines 40 through 44 can be interpreted as disclosing or suggesting that logic 400 is programmed to function as an HTTP manageability web server.

> *Cromer* at column 3, lines 44 through 47 states the following:
> The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

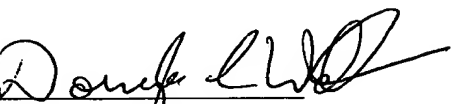
Cromer thus specifically teaches that logic 400 detects states, creates packets, and sends data over the MII bus to physical layer 304. This is the only functionality that *Cromer* discloses that is performed by logic 400. Nowhere does *Cromer* disclose or suggest that logic 400 is programmed to function as an HTTP manageability web server. In fact, nowhere does *Cromer* indicate that logic 400 is able to receive packets or any other communications over a network. Thus it is clear that *Cromer* does not disclose or suggest logic 400 is programmed to function as an HTTP manageability web server.

CONCLUSION

For all the reasons discussed above, Appellant believes the rejection of the claims was in error and respectfully requests that the rejection be reversed.

Respectfully submitted,

DAVE GOH, ET AL.

By 
Douglas L. Weller
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Appendix: Appealed Claims

1. A chip for incorporation within a network device connectable to a computer network, the network device including a host processor, the chip comprising:

a media access controller connectable to the computer network, the media access controller providing the chip with access to the computer network independent of the host processor;

a host interface connectable to the host processor; and

an embedded processor coupled between the host interface and the media access controller;

the embedded processor being programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device;

the embedded processor further being programmable to send the manageability information to the media access controller for transmission over the computer network;

whereby the chip performs network management functions independent of the host processor.

2. The chip of claim 1, wherein the embedded processor is programmable to obtain the manageability information in response to a network request addressed to the manageability web server.

3. The chip of claim 1, the network device further including an interchip communications means and a compliant device coupled to the interchip communication means, wherein the chip includes an interface connectable to the interchip communications means, and wherein the embedded processor is programmable to communicate via the interchip communication means interface to obtain manageability information about the compliant device.

4. The chip of claim 3, wherein the interchip communication means includes an I^2C bus, and wherein the compliant device is an I^2C-compliant device.

5. The chip of claim 3, wherein the embedded processor is also programmable to control the compliant device coupled to the interchip communications means.

6. The chip of claim 5, wherein the compliant device is a power supply controller, and wherein the embedded processor is programmable to control the power supply controller.

7. The chip of claim 5, wherein the compliant device is a fan controller, and wherein the embedded processor is programmable to control the fan controller.

8. The chip of claim 5, wherein the embedded processor is programmable to control the compliant device in response to a network request addressed to the manageability web server.

9. The chip of claim 5, wherein the embedded processor is programmable to perform firmware upgrades of the network device.

10. The chip of claim 1, wherein the embedded processor is programmable to perform network communications using TCP/IP.

11. The chip of claim 1, wherein the embedded processor is programmable to implement an HTTP web server.

12. The chip of claim 1, wherein the embedded processor is programmable to obtain manageability information from the host processor.

13. A network device connectable to a computer network, the network device comprising:

interchip communications means;

a compliant device coupled to the interchip communications means;

a chip including a media access controller connectable to the computer network; an interchip communications interface connected to the interchip communications means; and an embedded processor coupled to the interchip communications interface and the media access controller; and

non-volatile memory programmed with a plurality of executable instructions, the instructions, when executed, instructing the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network.

14. The network device of claim 13, wherein the instructions instructs the embedded processor to obtain the manageability information from the compliant device in response to network requests addressed to the manageability web server.

15. The network device of claim 13, further comprising a host processor; wherein the chip includes a host interface coupled to the host processor and the embedded processor, and wherein the instructions instruct the embedded processor to obtain manageability information from the host processor.

16. The network device of claim 13, wherein the interchip communications means includes an I^2C bus, wherein the compliant device is an I^2C- compliant device, and wherein the instructions instruct the embedded processor to control the I^2C-compliant device in response to network requests addressed to the manageability web server.

17. The network device of claim 16, wherein the I^2C-compliant device is a power supply controller, and wherein the instructions instruct the embedded processor to control the power supply controller,

18. The network device of claim 16, wherein the I^2C-compliant device is a fan controller, and wherein the instructions instruct the embedded processor to control the fan controller.

19. The device of claim 13, wherein the non-volatile memory further stores web page content.

20. The device of claim 13, further comprising volatile memory for storing the manageability information.

21. The device of claim 13, wherein the instructions instruct the embedded processor to perform network communications using TCP/IP.

22. The device of claim 13, wherein the instructions instruct the embedded processor to implement an HTTP web server.

23. (Previously presented) A system comprising:

a computer network;

a network device including a host processor and a chip, the chip including

a media access controller coupled to the computer network, and

an embedded processor coupled to the media access controller and programmed to function as an HTTP manageability web server; and

a network manager coupled to the computer network, the network manager including a web browser and a plurality of HTML files for instructing the network manager to communicate with the embedded processor in the network device and perform network management of the network device;

whereby the embedded processor can communicate with the network manager independent of the host processor.

24. The system of claim 23, wherein the network device includes a compliant device and wherein the embedded processor is programmable to

control the compliant device in response to control requests from the network manager.

25. The system of claim 24, wherein the compliant device is a fan controller, and wherein the network manager can request the embedded processor to control the fan controller to adjust fan speed.

26. The system of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to shut down and turn on the network device at scheduled times.

27. The system of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to reboot the computer.

28. The system of claim 24, wherein the network device further includes an upgradable BIOS; and wherein the network manager can send a BIOS upgrade program to the embedded processor and request the embedded processor to run the BIOS upgrade program.

29. The system of claim 24, wherein the network manager can send a diagnostic program to the embedded processor and request the embedded processor to run the diagnostic program and return to the network manager results obtained by the diagnostic program.

30. The system of claim 23, wherein the embedded processor is programmable to communicate with host interface and obtain manageability information from the host processor in response to requests by the network manager.

EVIDENCE APPENDIX

No evidence under §§ 1.130, 1.131, or 1.132 is relied upon by Appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

There are no related decisions rendered by a court or the Board.